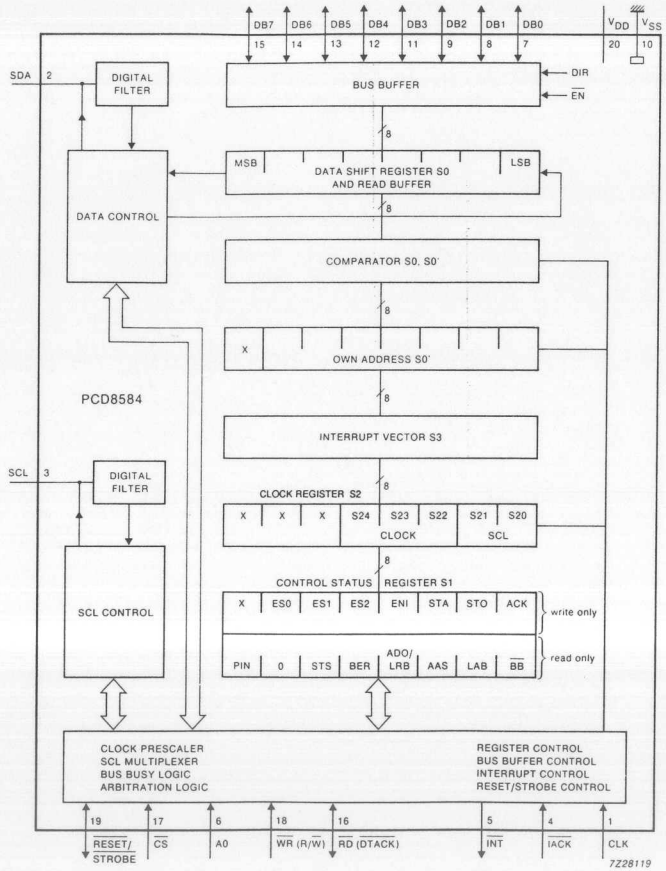
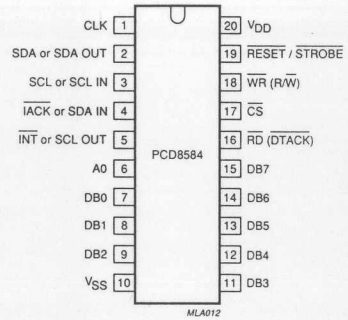


Where:

( ) indicate the SCN68000 pin name designations.
X = don't care.

Fig.1 Block diagram.

PINNING



Where:

( ) indicate the SCN68000 pin name designations.

Fig.2 Pinning diagram.

Pin functions

pin	mnemonic	function	description
1	CLK	I	Clock input from microprocessor clock generator (internal pull-up).
2	SDA or SDA OUT	I/O	I²C-bus serial data input/output (open-drain). Serial data output in long-distance mode.
3	SCL or SCL IN	I/O	I²C-bus serial clock input/output (open-drain). Serial clock input in long-distance mode.
4	$\overline{IACK}$ or SDA IN	I	Interrupt acknowledge input (internal pull-up); when this signal is asserted the interrupt vector in Register S2 will be available at the bus port if the ENI flag is set. Serial data input in long-distance mode.
5	$\overline{INT}$ or SCL OUT	O	Interrupt output (open-drain); this signal is enabled by the ENI flag in Register S1. It is asserted, when the PIN flag is reset. (PIN is reset after one byte is transmitted or received over the I²C-bus). Serial clock output in long-distance mode.
6	A0	I	Register select input (internal pull-up); this input selects between the control/status register and the other registers. Logic 1 selects Register S1, logic 0 selects one of the other registers depending on bits loaded in ES0, ES1 and ES2 of Register S1.
7	DB0	I/O	
8	DB1	I/O	Bidirectional 8-bit bus port.
9	DB2	I/O	
10	V_{SS}		Negative supply voltage.

Pin functions (continued)

pin	mnemonic	function	description
11	DB3	I/O	
12	DB4	I/O	
13	DB5	I/O	Bidirectional 8-bit bus port.
14	DB6	I/O	
15	DB7	I/O	
16	$\overline{RD}$ ($\overline{DTACK}$)	I (O)	$\overline{RD}$ is the read control input for MAB8049, MAB8051 or Z80-type processors. $\overline{DTACK}$ is the data transfer control output for 68000-type processors (open-drain).
17	$\overline{CS}$	I	Chip select input (internal pull-up).
18	$\overline{WR}$ (R/$\overline{W}$)	I	$\overline{WR}$ is the write control input for MAB8048, MAB8051 or Z80-type processors (internal pull-up). R/$\overline{W}$ control input for 68000-type processors.
19	$\overline{RESET}$/ $\overline{STROBE}$	I/O	Reset input (open-drain); this input forces the I²C-bus controller into a predefined state; all flags are reset, except PIN, which is set. Also functions as strobe output.
20	V_{DD}		Positive supply voltage.

FUNCTIONAL DESCRIPTION

General

The PCD8584 acts as an interface device between standard high-speed parallel buses and the serial I²C-bus. On the I²C-bus, it can act either as master or slave. Bidirectional data transfer between the I²C-bus and the parallel-bus microprocessor is carried out on a byte-wise basis, using either an interrupt or polled handshake. Interface to either 80XX-type (e.g. MAB8048, MAB8051, Z80) or 68000-type buses is possible. Selection of bus type is automatically performed (see **Interface mode control**).

Table 1 Control signals utilized by the PCD8584 for processor interfacing

type	R/$\overline{W}$	$\overline{WR}$	$\overline{RD}$	$\overline{DTACK}$	$\overline{IACK}$
MAB8049/51	NO	YES	YES	NO	NO
SCC68000	YES	NO	NO	YES	YES
Z80	NO	YES	YES	NO	YES

The structure of the PCD8584 is similar to that of the I²C-bus interface section of the MAB8400-series of microcontrollers, but with a modified control structure. The PCD8584 has five internal register locations. Three of these (Own Address register S0', Clock register S2 and Interrupt Vector S3) are used for initialization of the PCD8584. Normally they are only written once directly after resetting of the PCD8584. The remaining two registers function as double registers (Data Buffer/Shift register S0, and Control/Status register S1) which are used during actual data transmission/reception. By using these double registers, which are separately write and read accessible, overhead for register access is reduced. S0 is a combination of a shift register and data buffer. S0 performs all serial-to-parallel interfacing with the I²C-bus. S1 contains I²C-bus status information required for bus access and/or monitoring.

FUNCTIONAL DESCRIPTION (continued)

Interface mode control (IMC)

Selection of either an 80XX-mode or 68000-mode interface is achieved by detection of the $\overline{WR}$ · $\overline{CS}$ signal sequence. The concept takes advantage of the fact that the write control input is common for both types of interfaces. The chip is non-initialized after reset until register S0' is accessed. An 80XX-type interface is default. If a HIGH-to-LOW transition of $\overline{WR}$ (R/$\overline{W}$) is detected while $\overline{CS}$ is HIGH, the 68000-type interface mode is selected and the $\overline{DTACK}$ output is enabled.

Note:

The very first access to the PCD8584 after a reset must be a write access to register S0' in order to set the appropriate interface mode.

Set-up Registers S0', S2 and S3

Own Address Register S0'

When addressed as a slave, this register is loaded with the 7-bit I²C-bus address to which the PCD8584 is to respond. The "Addressed As Slave" (AAS) bit in Status register S1 is set when this address is received. Programming of this register is accomplished via the parallel-bus when A0 is LOW, with the appropriate bit combinations set in Control Status register S1 (S1 is written when A0 is HIGH). Bit combinations for accessing all registers are given in Tables 4 and 5. After reset S0' has default address '00' Hex.

Clock Register S2

Register S2 provides control over chip clock frequency and SCL clock frequency. S20 and S21 provide a selection of 4 different I²C-bus SCL frequencies which are shown in Table 2.

Table 2 Register S2 selection of SCL frequency

bit S21	bit S20	SCL approximate frequency (kHz)
0	0	90
0	1	45
1	0	11
1	1	1.5

S22, S23 and S24 are used for control of the internal clock prescaler. Due to the possibility of varying microprocessor clock signals, the prescaler can be programmed to adapt to 5 different clock rates, thus providing a constant internal clock. This is required to provide a stable time base for the SCL generator and the digital filters associated with the I²C-bus signals SCL and SDA. Selection for adaption to external clock rates is shown in Table 3. After reset, a clock frequency of 12 MHz is the default value

Table 3 Register S2 selection of clock frequency

bit S24	bit S23	bit S22	clock frequency (MHz)
0	X	X	3
1	0	0	4.43
1	0	1	6
1	1	0	8
1	1	1	12

Where: X = don't care.

Interrupt Vector S3

The interrupt vector register provides an 8-bit user-programmable vector for vectored-interrupt microprocessors. The vector is sent to the bus port when an interrupt acknowledge signal is asserted and the ENI (enable interrupt) flag is set. Default vector values are as follows:

- Vector is '00' Hex in 80XX-mode
- Vector is '0F' Hex in 68000-mode

On reset the PCD8584 is in the 80XX mode, thus the default interrupt vector becomes '00' Hex.

Interface Registers S0 and S1

Data Shift Register S0

S0 acts as serial shift register interfacing to the I²C-bus. S0 is a combination of a shift register and a data buffer; parallel data is always written to the shift register and read from the data buffer. Serial data is shifted in/out the shift register, and in receiver mode the data from the shift register is copied to the data buffer during the acknowledge phase (see also PIN bit). All read and write operations to the I²C-bus are done via this register.

Control/Status Register S1

Register S1 is accessed by a HIGH signal on register select input A0. To facilitate communication between the microcontroller/processor and the I²C-bus, register S1 has separate read and write functions for all bit positions.

The write-only section has been split into 2 parts:

- The ESO (Enable Serial Output) enables or disables the serial output. When ESO is LOW, register access for initialization is possible. When ESO is HIGH, serial communication is enabled; communication with serial shift register S0 is enabled and the S1 bus status bits are made available for reading. Select control bits ES1 and ES2 control selection of other registers for initialization and control of normal operation. After these bits are programmed for access to the desired register (see Tables 4 and 5), the register is selected by a logic LOW level on register select pin A0.

Note:

With ESO = 0, bits ENI, STA, STO and ACK of S1 can be read for test purposes.

FUNCTIONAL DESCRIPTION (continued)

Control/Status Register S1 (continued)

Table 4 Register access control; ESO = logic 0 (serial interface off)

A0	ES1	ES1	$\overline{\text{IACK}}$	operation
H	X	X	X	READ/WRITE CONTROL REGISTER (S1) STATUS (S1) not available
L	0	0	X	READ/WRITE OWN ADDRESS (S0')
L	0	1	X	READ/WRITE INTERRUPT VECTOR (S3)
L	1	0	X	READ/WRITE CLOCK REGISTER (S2)

Table 5 Register access control; ESO = logic 1 (serial interface on)

A0	ES1	ES2	$\overline{\text{IACK}}$	operation
H	X	X	H	WRITE CONTROL REGISTER (S1)
H	X	X	H	READ STATUS REGISTER (S1)
L	X	0	H	READ/WRITE DATA (S0)
L	X	1	H	READ/WRITE INTERRUPT VECTOR (S3)
X	0	X	L	READ INTERRUPT VECTOR (acknowledge cycle)
X	1	X	L	long-distance mode

Instruction control bits ENI, STA, STO and ACK are used in normal operation to enable the interrupt output ($\overline{\text{INT}}$), generate I²C-bus START and STOP conditions, and program the acknowledge response, respectively. These possibilities are shown in Table 6.

Table 6 Instruction table for serial bus control

STA	STO	present mode	function	operation
1	0	SLV/REC	START	transmit START + address remain MST/TRM if R/$\overline{W}$ = logic 0; go to MST/REC if R/$\overline{W}$ = logic 1
1	0	MST/TRM	REPEAT START	same as for SLV/REC
0	1	MST/REC MST/TRM	STOP READ STOP WRITE	transmit stop go to SLV/REC mode (see note 1)
1	1	MST	DATA CHAINING	send STOP, START and address after last master frame without STOP sent (see note 2)
0	0	ANY	NOP	no operation (see note 3)

Notes to Table 6

1. In master-receiver mode, the last byte must be terminated with ACK bit HIGH ("negative-acknowledge"; see I²C-bus specification).
2. If both STA and STO are set HIGH simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows "chaining" of transmissions without relinquishing bus control.
3. All other STA, STO mode combinations not mentioned in Table 6 are NOPs.

The instruction bits are defined as follows:

- STA, STO: These bits control the generation of the I²C-bus START condition + transmission of slave address and R/$\overline{W}$ bit, generation of repeated START condition, and generation of the STOP condition.
- ENI: This bit enables the external interrupt output $\overline{INT}$, which is generated when the PIN bit is reset.
- ACK: This bit must be set normally to a '1'. This causes the I²C-bus controller to send an acknowledge automatically after each byte (this occurs during the ninth clock pulse). The bit must be reset when the I²C-bus controller is operating in master/receiver mode, and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the I²C-bus, which halts further transmission from the slave device.

FUNCTIONAL DESCRIPTION (continued)

I²C-bus status information

The read-only section consists of I²C-bus status information. The functions are as follows:

- STS: When in slave-receiver mode, this flag is asserted when an externally generated STOP condition is detected (only used in slave-receiver mode).
- BER: Bus error. A misplaced START or STOP condition has been detected.
- LRB/AD0: Last Received Bit/Address 0 "General Call" Bit. This dual function status bit holds the value of the last received bit over the I²C-bus when AAS = 0. Normally this will be the value of the slave acknowledge; thus checking for slave acknowledgment is done via testing of the LRB bit. When AAS = 1 ("Address As Slave"), the I²C-bus controller has been addressed as a slave and this bit will be set if the slave address received was the "general call" address, or if it was the I²C-bus controller's slave address.
- AAS: "Addressed As Slave" bit. When acting as slave-receiver, this flag is set when an incoming address over the I²C-bus matches the value in Own Address register S0', or if the I²C-bus "general call" address ("00" Hex) has been received.
- LAB: "Lost Arbitration" bit. This bit is set when, in multmaster operation, arbitration is lost to another master on the I²C-bus.
- $\overline{BB}$: "Bus Busy" bit. This is read-only flag indicating when the I²C-bus is in use. A zero indicated that the bus is busy, and access is not possible. This bit is set/reset by STOP/START conditions.

PIN bit

The PIN bit "Pending Interrupt Not" is a read-only flag which is used to synchronize serial communication. Each time a serial data transmission is initiated (by setting the STA bit in the same register), the PIN will be set automatically. After successful transmission of one byte (9 clock pulses, including acknowledge) this bit will be automatically reset indicating a complete byte transmission. When the ENI bit is also set the PIN flag triggers an external interrupt via the $\overline{INT}$ output when PIN is reset. When in receiver mode the PIN bit is also reset on completion of each received byte. In polled applications, the PIN bit is tested to determine when a serial transmission has been completed. During register transfers the I²C-bus controller Data Register S0 and its internal shift register (not accessible directly), the I²C-bus controller will delay serial transmission by holding the SCL line LOW until the PIN bit becomes set. In receiver mode, the PIN bit is automatically set when the data register S0 is read. When the PIN bit becomes set all status bits will be reset, with exception of $\overline{BB}$.

Multi-master operations

To avoid conflict between data and repeated START and STOP operations, multi-master systems have some limitations:

- Transmissions requiring a repeated START condition must have identical format among all potential masters for both read and write operations
- For correct arbitration masters may only attempt to send data simultaneously to the same location if they use the same formats (i.e. number of data bytes, location of the repeated START, etc.). If this condition is designed not to occur, differing formats may be used.

Reset A low-level pulse on the $\overline{RESET}$ input forces the I²C-bus controller into a well-defined state. All flags are reset (zero state), except the PIN flag, which is set. The $\overline{RESET}$ pin is also used for the $\overline{STROBE}$ output signal. Both functions are separated on-chip by a digital filter. The reset input signal has to be sufficiently long (minimum 30 clock cycles) to pass through the filter. The $\overline{STROBE}$ output signal is sufficiently short (8 clock cycles) to be blocked by the filter. For more detailed information on the Strobe function see **Special function modes.**

FUNCTIONAL DESCRIPTION (continued)

Comparison to the MAB8400 I²C-bus interface

The structure of the PCD8584 is similar to that of the MAB8400 series of microcontrollers, but with a modified control structure. Access to all I²C-bus control and status registers is done via the parallel-bus port in conjunction with register select input A0, and control bits ESO, ES1 and ES2. The main differences are highlighted below.

Deleted functions

The following functions are not available in the PCD8584:

- Always selected (ALS flag)
- Access to the bit counter (BC0 to BC2)
- Full SCL frequency selection (2 bits instead of 5 bits)
- The non-acknowledge mode (ACK flag)
- Asymmetrical clock (ASC flag)

Added functions

The following functions either replace the deleted functions or are completely new:

- Chip clock prescaler
- Assert acknowledge bit (ACK flag)
- Register selection bits (ES1 and ES2 flags)
- Additional status flags
- Automatic interface control between 80XX and 68000-type microprocessors
- Programmable interrupt vector
- Strobe generator
- Bus monitor function
- Long-distance mode (non-I²C-bus mode; only for communication between remote parallel-bus processors)

Special function modes

Strobe

When the I²C-bus controller receives its own address (or the "00" Hex general call address) followed immediately by a STOP condition (i.e. no further data transmitted after the address), a strobe output signal is generated at the $\overline{\text{RESET}}/\overline{\text{STROBE}}$ pin (pin 19). The $\overline{\text{STROBE}}$ signal consists of a monostable output pulse (active LOW), eight clock cycles long (see Fig.10). It is generated after the STOP condition is received, preceded by the correct slave address. This output can be used as a bus access controller for multi-master parallel-bus systems (see Fig.14).

Long-distance mode

The long-distance mode provides a serial communication link between parallel processors using two or more I²C-bus controllers. This mode is selected by setting ES1 to logic 1 while the serial interface is enabled (ESO = 1). In this mode the I²C-bus protocol is transmitted over 4 unidirectional lines, SDA, OUT, SCL IN, SDA IN and SCL OUT (pins 2, 3, 4 and 5). These communication lines should be connected to the line drivers/receivers for long distance applications. Specification for long distance transmission is then given by the chosen standard. Control of bus frequency, data transmission etc. is the same as in normal I²C-bus mode. After reading or writing data to shift register S0, long-distance mode must be initialized by setting ESO and ES1 to logic 1. Because the interrupt output $\overline{\text{INT}}$ is not available in this operating mode, data reception must be polled.

Monitor mode

When the 7-bit Own Address register S0' is loaded with all zeros, the I²C-bus controller acts as a passive I²C monitor. The main features of the monitor mode are as follows:

- The controller is always selected
- The controller is always in the slave-receiver mode
- The controller never generates an acknowledge
- The controller never generates an interrupt request
- A pending interrupt condition does not force SCL LOW
- Received data is automatically transferred to the read buffer
- Bus traffic is monitored by the PIN bit, which is reset after the acknowledge bit has been transmitted and is set as soon as the first bit of the next byte is detected

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 20)	V_{DD}	−0.3	+ 7.0	V
Voltage range on any input*	V_I	−0.8	V_{DD} + 0.5	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Total power dissipation	P_{tot}	–	300	mW
Power dissipation per output	P_O	–	50	mW
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

Note to the Ratings

Stresses above those listed in accordance with Absolute Maximum System may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 5 ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4.5	5.0	5.5	V
Supply current						
standby	note 1	I_{DD1}	–	–	2.5	μA
operating	note 2	I_{DD2}	–	–	1.5	mA
Inputs						
SCL, SDA						
Input voltage LOW	note 3	V_{IL1}	0	–	0.8	V
Input voltage HIGH	note 3	V_{IH1}	2.0	–	V_{DD}	V
Input voltage LOW	note 4	V_{IL2}	0	–	$0.3V_{DD}$	V
Input voltage HIGH	note 4	V_{IH2}	$0.7V_{DD}$	–	V_{DD}	V
Resistance to V_{DD}	T_{amb} = 25 °C; note 5	R_i	25	–	100	kΩ
Outputs						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3.0	–	–	mA
Output current HIGH	V_{OH} = 2.4 V; note 6	$-I_{OH}$	2.4	–	–	mA
Leakage current	note 7	$\pm I_{LO}$	–	–	1	μA

Notes to the characteristics

1. 22 kΩ pull-ups on D0 to D7; 10 kΩ pull-ups on SDA, SCL, $\overline{RD}$; $\overline{RESET}$ tied to V_{SS}; remaining pins open-circuit.
2. Same as note 1, but CLK waveform with 50% duty factor at 12 MHz.
3. CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$, TTL level inputs.
4. SDA, SCL, D0 to D7, CMOS level inputs.
5. CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$.
6. D0 to D7.
7. D0 to D7 3-state, SDA, SCL, $\overline{INT}$, $\overline{RD}$, $\overline{RESET}$.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
I²C-bus timing					
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable bus spike width	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

Parallel interface timing (see Figs 3 to 10)

All the timing limits are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
C_L = 100 pF, R_L = 1.5 kΩ (connected to V_{DD}) for open-drain and high-impedance outputs, where applicable (for measurement purposes only).

parameter	figure	symbol	min.	typ.	max.	unit
Clock rise time	3	t_r	–	–	6	ns
Clock fall time	3	t_f	–	–	6	ns
Input clock period (50% duty factor)	3	t_{CLK}	83	–	333	ns
$\overline{CS}$ set-up to $\overline{RD}$, $\overline{WR}$ LOW	4	t_{SU1}	30	–	–	ns
$\overline{CS}$ hold from $\overline{RD}$, $\overline{WR}$ HIGH	4	t_{HD1}	0	–	–	ns
A0 set-up to $\overline{RD}$, $\overline{WR}$ LOW	4	t_{SU2}	10	–	–	ns
A0 hold from $\overline{RD}$, $\overline{WR}$ HIGH	4	t_{HD2}	20	–	–	ns
$\overline{WR}$ pulse width	4	t_{W1}	230	–	–	ns
$\overline{RD}$ pulse width	4	t_{W2}	230	–	–	ns
Data set-up before $\overline{WR}$ HIGH	4	t_{SU3}	150	–	–	ns
Data valid after $\overline{RD}$ LOW	4	t_{VD}	–	110	180	ns
Data hold after $\overline{WR}$ HIGH	4	t_{HD3}	30	–	–	ns
Data bus floating after $\overline{RD}$ HIGH	4	t_{FL}	70	–	–	ns
A0 set-up to $\overline{CS}$ LOW	5 and 6	t_{SU4}	30	–	–	ns
R/$\overline{WR}$ set-up to $\overline{CS}$ LOW	5 and 6	t_{SU5}	30	–	–	ns
Data valid after $\overline{CS}$ LOW	5	t_{VD1}	–	110	180	ns
$\overline{DTACK}$ LOW after $\overline{CS}$ LOW	5 and 6	t_{d1}	–	$3t_{CLK}+75$	$3t_{CLK}+150$	ns
A0 hold from $\overline{CS}$ HIGH	5 and 6	t_{HD4}	0	–	–	ns
R/$\overline{WR}$ hold from $\overline{CS}$ HIGH	5 and 6	t_{HD5}	0	–	–	ns
Data hold after $\overline{CS}$ HIGH	5	t_{HD6}	160	–	–	ns
$\overline{DTACK}$ HIGH from $\overline{CS}$ HIGH	5 and 6	t_{d2}	–	100	120	ns
Data hold after $\overline{CS}$ HIGH	6	t_{HD7}	0	–	–	ns
Data set-up to $\overline{CS}$ LOW	6	t_{SU6}	0	–	–	ns
$\overline{INT}$ HIGH from $\overline{IACK}$ LOW	7 and 8	t_{d3}	–	130	180	ns
Data valid after $\overline{IACK}$ LOW	7 and 8	t_{VD2}	–	140	190	ns

Parallel interface timing (continued)

parameter	figure	symbol	min.	typ.	max.	unit
$\overline{IACK}$ pulse width	7 and 8	t_{W3}	230	–	–	ns
Data hold after $\overline{IACK}$ HIGH	7 and 8	t_{HD8}	100	–	–	ns
$\overline{DTACK}$ LOW from $\overline{IACK}$ LOW	8	t_{d4}	–	$3t_{CLK}+75$	$3t_{CLK}+150$	ns
$\overline{DTACK}$ HIGH from $\overline{IACK}$ HIGH	8	t_{d5}	–	120	140	ns
Reset pulse width	9	t_{W4}	$30t_{CLK}$	–	–	ns
Strobe pulse width	10	t_{W5}	$8t_{CLK}$	$8t_{CLK}+90$	–	ns

Notes to parallel interface timing

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses when the I²C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. After reset the chip clock default is 12 MHz.

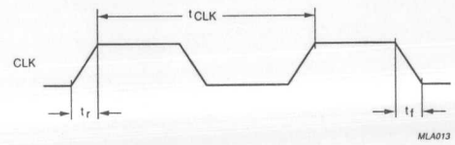
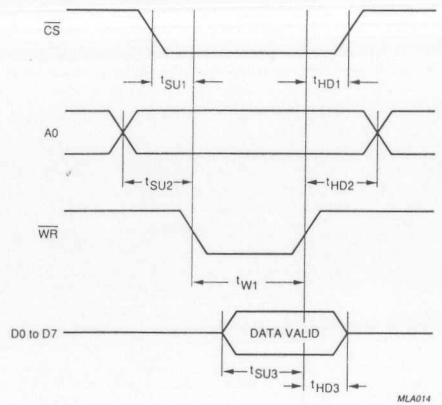
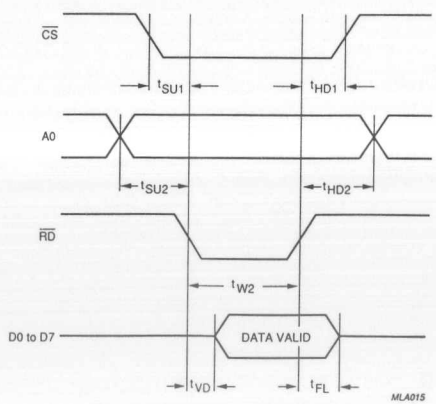


Fig.3 Clock input timing.

Timing diagrams



(a)



(b)

Fig. 4 Bus timing (80XX-mode); (a) write cycle, (b) read cycle.

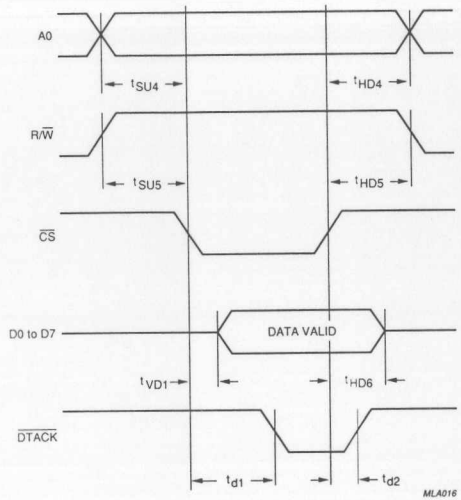


Fig.5 Bus timing; 68000-mode read cycle.

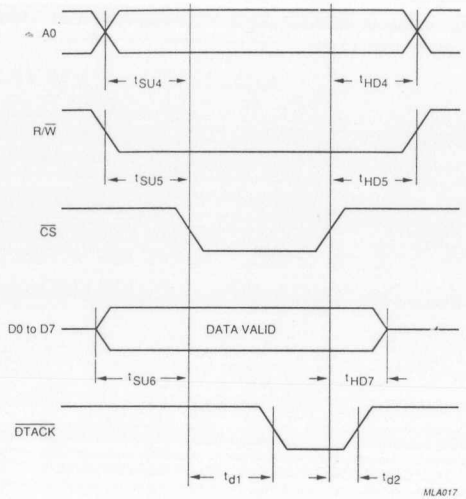


Fig.6 Bus timing; 68000-mode write cycle.

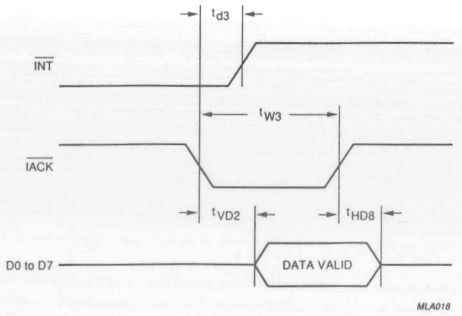


Fig.7 Interrupt timing; 80XX-mode.

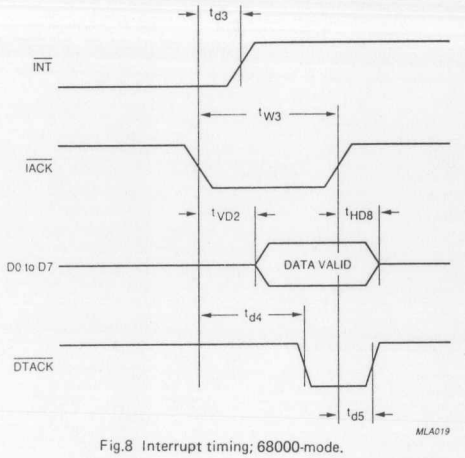


Fig.8 Interrupt timing; 68000-mode.

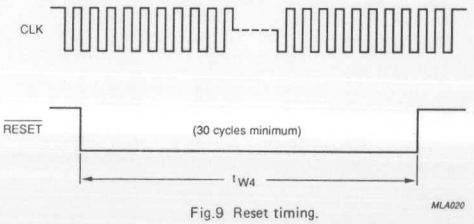


Fig.9 Reset timing.

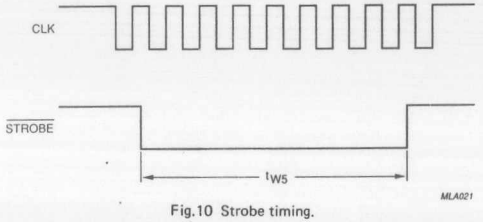


Fig.10 Strobe timing.

APPLICATION INFORMATION

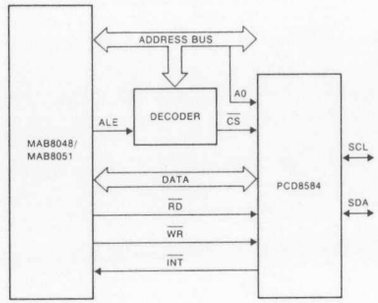


Fig.11 Application diagram using the MAB8048/MAB8051.

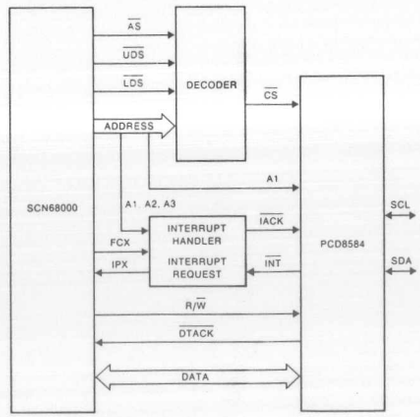


Fig.12 Application diagram using the SCN68000.

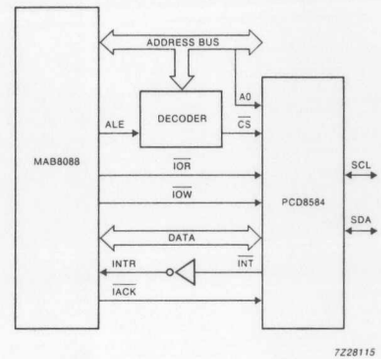


Fig.13 Application diagram using the 8088.

APPLICATION INFORMATION (continued)

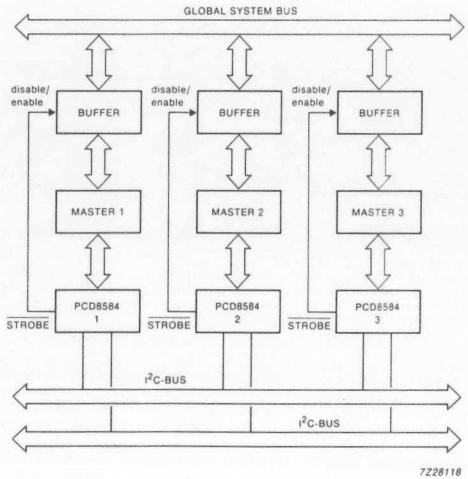


Fig.14 $\overline{\text{STROBE}}$ as bus access controller.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Universal LCD driver for low multiplex rates PCF8566

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I²C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).